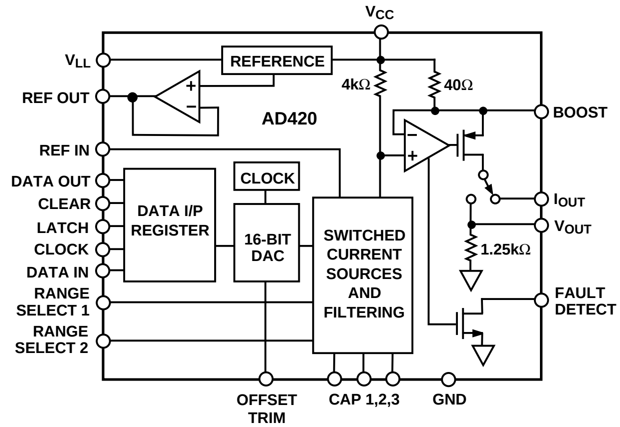
Serial Input 16-Bit 4–20 mA, 0–20 mA DAC

AD420

FEATURES
4–20 mA, 0–20 mA or 0–24 mA Current Output
16-Bit Resolution and Monotonicity
±0.012% max Integral Nonlinearity
±0.05% max Offset (Trimmable)
±0.15% max Total Output Error (Trimmable)
Flexible Serial Digital Interface (3.3 MBPS)
On-Chip Loop Fault Detection
On-Chip 5 V Reference (25 ppm/°C max)
Asynchronous CLEAR Function
Maximum Power Supply Range of 32 V
Output Loop Compliance of 0 V to V_{CC} – 2.5 V
24-Pin SOIC and PDIP Packages

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD420 is a complete digital to current loop output converter, designed to meet the needs of the industrial control market. It provides a high precision, fully integrated, low cost single-chip solution for generating current loop signals in a compact 24-pin SOIC or PDIP package.

The output current range can be programmed to 4 mA–20 mA, 0 mA–20 mA or an overrange function of 0 mA–24 mA. The AD420 can alternatively provide a voltage output from a separate pin that can be configured to provide 0 V–5 V, 0 V–10 V, ±5 V or ±10 V with the addition of a single external buffer amplifier.

The 3.3M Baud serial input logic design minimizes the cost of galvanic isolation and allows for simple connection to commonly used microprocessors. It can be used in three-wire or asynchronous mode and a serial-out pin is provided to allow daisy chaining of multiple DACs on the current loop side of the isolation barrier.

The AD420 uses sigma-delta (ΣΔ) DAC technology to achieve 16-bit monotonicity at very low cost. Full-scale settling to 0.1% occurs within 3 ms. The only external components that are required (in addition to normal transient protection circuitry) are three low cost capacitors which are used in the DAC output filter.

If the AD420 is going to be used at extreme temperatures and supply voltages, an external output transistor can be used to minimize power dissipation on the chip via the "BOOST" pin.

The FAULT DETECT pin signals when an open circuit occurs in the loop. The on-chip voltage reference can be used to supply a precision +5 V to external components in addition to the AD420 or, if the user desires temperature stability exceeding 25 ppm/°C, an external precision reference such as the AD586 can be used as the reference.

The AD420 is available in a 24-pin SOIC and PDIP over the industrial temperature range of –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. The AD420 is a single chip solution for generating 4 mA–20 mA or 0 mA–20 mA signals at the "controller end" of the current loop.
2. The AD420 is specified with a power supply range from 12 V to 32 V. Output loop compliance is 0 V to V_{CC} – 2.5 V.
3. The flexible serial input can be used in three-wire mode with SPI* or MICROWIRE† microcontrollers, or in asynchronous mode which minimizes the number of control signals required.
4. The serial data out pin can be used to daisy chain any number of AD420s together in three-wire mode.
5. At power-up the AD420 initializes its output to the low end of the selected range.
6. The AD420 has an asynchronous CLEAR pin which sends the output to the low end of the selected range (0 mA, 4 mA, or 0 V).
7. The AD420 BOOST pin accommodates an external transistor to off-load power dissipation from the chip.
8. The offset of ±0.05% and total output error of ±0.15% can be trimmed if desired, using two external potentiometers.

*SPI is a registered trademark of Motorola.
†MICROWIRE is a registered trademark of National Semiconductor.

REV. C

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AD420–SPECIFICATIONS ($T_A = T_{MIN}–T_{MAX}$, V_{CC} = + 24 V, R_L = 500 Ω, unless otherwise noted)

Parameter	AX-32 Versions[1] Min	Typ	Max	Units	Comments
RESOLUTION	16			Bits	
ACCURACY[2]					
Monotonicity	16			Bits	
Integral Nonlinearity		±0.002	±0.012	%	
Offset (0 mA or 4 mA) (T_A = +25°C)			±0.05	%	
Offset Drift		20	50	ppm/°C	
Total Output Error (20 mA or 24 mA) (T_A = +25°C)			±0.15	%	
Total Output Error Drift		20	50	ppm/°C	
PSRR[3]		5	10	μA/V	
OUTPUT CHARACTERISTICS					
Operating Current Ranges	4		20	mA	
	0		20	mA	
	0		24	mA	
Current Loop Voltage Compliance	0		V_{CC} – 2.5 V	V	
Output Voltage Range (Pin 17)	0		5	V	
Settling Time (to 0.1% of FS)[4]		2.5	3	ms	
Output Impedance (Current Mode)		25		MΩ	
VOLTAGE REFERENCE					
REF OUT					
Output Voltage (T_A = +25°C)	4.995	5.0	5.005	V	
Drift			±25	ppm/°C	
Externally Available Current		5		mA	
Short Circuit Current		7		mA	
REF IN					
Resistance		30		kΩ	
V_{LL}					
Output Voltage		4.5		V	
Externally Available Current		5		mA	
Short Circuit Current		20		mA	
DIGITAL INPUTS					
V_{IH} (Logic 1)	2.4			V	
V_{IL} (Logic 0)			0.8	V	
I_{IH} (V_{IN} = 5.0 V)			±10	μA	
I_{IL} (V_{IN} = 0 V)			±10	μA	
Data Input Rate ("3-Wire" Mode)	No Minimum		3.3	MBPS	
Data Input Rate ("Asynchronous" Mode)	No Minimum		150	kBPS	
DIGITAL OUTPUTS					
FAULT DEFECT					
V_{OH} (10 kΩ Pull-Up Resistor to V_{LL})	3.6	4.5		V	
V_{OL} (10 kΩ Pull-Up Resistor to V_{LL})		0.2	0.4	V	
V_{OL} @ 2.5 mA		0.6		V	
DATA OUT					
V_{OH} (I_{OH} = –0.8 mA)	3.6	4.3		V	
V_{OL} (I_{OL} = 1.6 mA)		0.3	0.4	V	
POWER SUPPLY					
Operating Range V_{CC}	12		32	V	
Quiescent Current		4.2	5.0	mA	
Quiescent Current (External V_{LL})		3		mA	
TEMPERATURE RANGE					
Specified Performance	–40		+85	°C	

NOTES

[1]X refers to the package designator, R or N.

[2]Total Output Error includes Offset and Gain Error. Total Output Error and Offset Error are with respect to the Full-Scale Output and are measured with an ideal +5 V reference. If the internal reference is used, the reference errors must be added to the Offset and Total Output Errors.

[3]PSRR is measured by varying V_{CC} from 12 V to its maximum 32 V.

[4]External capacitor selection must be as described in Figure 5.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to GND
  AD420AR/AN-32 . . . . 32 V
I_{OUT} to GND . . . . V_{CC}
Digital Inputs to GND . . . . –0.5 V to +7 V
Digital Output to GND . . . . –0.5 V to V_{LL} + 0.3 V
V_{LL} and REF OUT: Outputs Safe for Indefinite Short to Ground.
Storage Temperature . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . +300°C
Thermal Impedance:
  SOIC (R) Package . . . . θ_{JA} = 75°C/W
  PDIP (N) Package . . . . θ_{JA} = 50°C/W

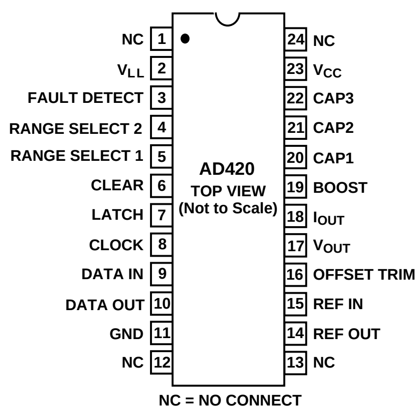
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Max Operating Voltage	Package Option*
AD420AN-32	–40°C to +85°C	32 V	N-24
AD420AR-32	–40°C to +85°C	32 V	R-24

*N = Plastic DIP, R = Plastic SOIC.

PIN DESIGNATIONS



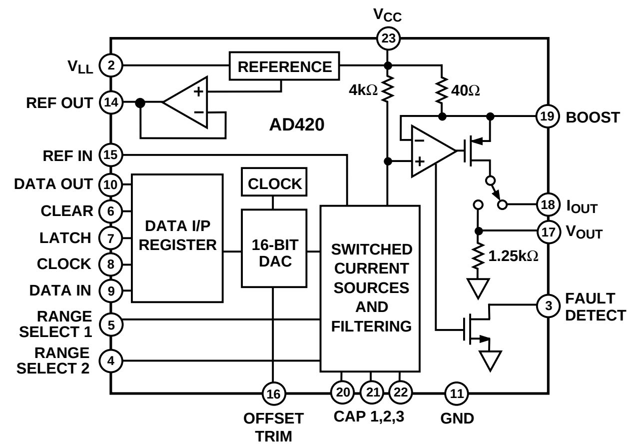


Figure 1. Functional Block Diagram

Table I. Truth Table

Inputs			
CLEAR	**Range Select 2**	**Range Select 1**	**Operation**
0	X	X	Normal Operation
1	X	X	Output at Bottom of Span
X	0	0	0 V–5 V Range
X	0	1	4 mA–20 mA Range
X	1	0	0 mA–20 mA Range
X	1	1	0 mA–24 mA Range

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD420 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Timing Requirements (T_A = –40°C to +85°C, V_{CC} = +12 V to +32 V)

THREE-WIRE INTERFACE

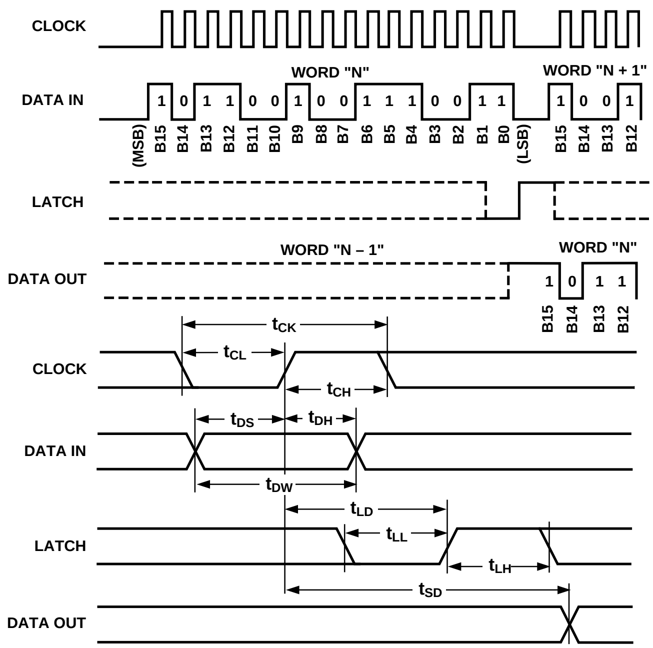


Figure 2. Timing Diagram for Three-Wire Interface

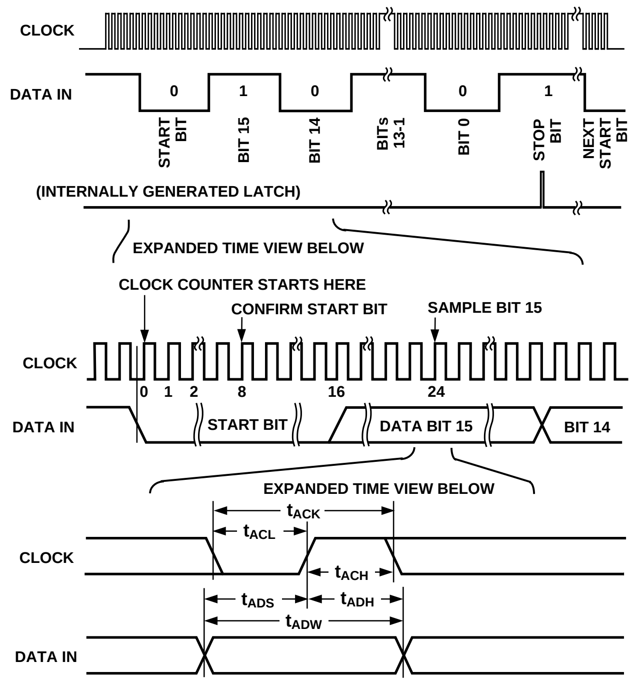


Figure 3. Timing Diagram for Asynchronous Interface

Table II. Timing Specification for Three-Wire Interface

Parameter	Label	Limit	Units
Data Clock Period	t_{CK}	300	ns min
Data Clock Low Time	t_{CL}	80	ns min
Data Clock High Time	t_{CH}	80	ns min
Data Stable Width	t_{DW}	125	ns min
Data Setup Time	t_{DS}	40	ns min
Data Hold Time	t_{DH}	5	ns min
Latch Delay Time	t_{LD}	80	ns min
Latch Low Time	t_{LL}	80	ns min
Latch High Time	t_{LH}	80	ns min
Serial Output Delay Time	t_{SD}	225	ns max
Clear Pulse Width	t_{CLR}	50	ns min

Table III. Timing Specifications for Asynchronous Interface

Parameter	Label	Limit	Units
Asynchronous Clock Period	t_{ACK}	400	ns min
Asynchronous Clock Low Time	t_{ACL}	50	ns min
Asynchronous Clock High Time	t_{ACH}	150	ns min
Data Stable Width (Critical Clock Edge)	t_{ADW}	300	ns min
Data Setup Time (Critical Clock Edge)	t_{ADS}	50	ns min
Data Hold Time (Critical Clock Edge)	t_{ADH}	20	ns min
Clear Pulse Width	t_{CLR}	50	ns min

ASYNCHRONOUS INTERFACE

Note in the timing diagram for asynchronous mode operation each data word is "framed" by a START (0) bit and a STOP (1) bit. The data timing is with respect to the rising edge of the CLOCK at the center of each bit cell. Bit cells are 16 clocks long, and the first cell (the START bit) begins at the first clock following the leading (falling) edge of the START bit. Thus the MSB (D15) is sampled 24 clock cycles after the beginning of the START bit, D14 is sampled at clock number 40, and so on. During any "dead time" before writing the next word the DATA IN pin must remain at logic 1.

The DAC output updates when the STOP bit is received. In the case of a "framing error" (the STOP bit sampled as a 0) the AD420 will output a pulse at the DATA OUT pin one clock period wide during the clock period subsequent to sampling the STOP bit. The DAC output will not update if a "framing error" is detected.

PIN DESCRIPTION

Pin #	Symbol	Function
2	V_{LL}	Auxiliary buffered +4.5 V digital logic voltage. This pin is the internal supply voltage for the digital circuitry and can be used as a termination for pull-up resistors. An external +5 V power supply can be connected to V_{LL}. It will override this buffered voltage, thus reducing the internal power dissipation.
3	FAULT DETECT	FAULT DETECT, connected to a pull-up resistor, is asserted low when the output current does not match the DAC's programmed value, for example, in case the current loop is broken.
4 5	RANGE SELECT 2 RANGE SELECT 1	Selects the converter's output operating range. One output voltage range and three output current ranges are available.
6	CLEAR	Valid V_{IH} will unconditionally force the output to go to the minimum of its programmed range. After CLEAR is removed the DAC output will remain at this value. The data in the input register is unaffected.
7	LATCH	In the three-wire interface mode a rising edge parallel loads the serial input register data into the DAC. To use the asynchronous mode connect LATCH through a current limiting resistor to V_{CC}.
8	CLOCK	Data Clock Input. The clock period is equal to the input data bit rate in the three-wire interface mode and is 16 times the bit rate in asynchronous mode.
9	DATA IN	Serial Data Input.
10	DATA OUT	Serial Data Output. In the three-wire interface mode, this output can be used for daisy-chaining multiple AD420s. In the asynchronous mode a positive pulse will indicate a framing error after the stop-bit is received.
11	GND	Ground (Common).
14	REF OUT	+5 V Reference Output.
15	REF IN	Reference Input.
16	OFFSET TRIM	Offset Adjust.
17	V_{OUT}	Voltage Output.
18	I_{OUT}	Current Output.
19	BOOST	Connect to an external transistor to reduce the power dissipated in the AD420 output transistor, if desired.
20 21 22	CAP 1 CAP 2 CAP 3	These pins are used for internal filtering. Connect capacitors between each of these pins and V_{CC}. Refer to the description of current output operation.
23	V_{CC}	Power Supply Input.
1, 12, 13, 24	NC	No Connection. No internal connections inside device.

DEFINITIONS OF SPECIFICATIONS

RESOLUTION: For 16-bit resolution, 1 LSB = 0.0015% of the FSR. In the 4 mA–20 mA range 1 LSB = 244 nA.

INTEGRAL NONLINEARITY: Analog Devices defines integral nonlinearity as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to FS – 1 LSB) for any bit combination. This is also referred to as relative accuracy.

DIFFERENTIAL NONLINEARITY: Differential nonlinearity is the measure of the change in the analog output, normalized to full scale, associated with an LSB change in the digital input code. Monotonic behavior requires that the differential linearity error be greater than –1 LSB over the temperature range of interest.

MONOTONICITY: A DAC is monotonic if the output either increases or remains constant for increasing digital inputs with the result that the output will always be a single-valued function of the input.

GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out.

OFFSET ERROR: Offset error is the deviation of the output current from its ideal value expressed as a percentage of the full-scale output with all 0s loaded in the DAC.

DRIFT: Drift is the change in a parameter (such as gain and offset) over a specified temperature range. The drift temperature coefficient, specified in ppm/°C, is calculated by measuring the parameter at T_{MIN}, 25°C, and T_{MAX} and dividing the change in the parameter by the corresponding temperature change.

CURRENT LOOP VOLTAGE COMPLIANCE: The voltage compliance is the maximum voltage at the I_{OUT} pin for which the output current will be equal to the programmed value.

THEORY OF OPERATION

The AD420 uses a sigma-delta (ΣΔ) architecture to carry out the digital-to-analog conversion. This architecture is particularly well suited for the relatively low bandwidth requirements of the industrial control environment because of its inherent monotonicity at high resolution.

In the AD420 a second order modulator is used to keep complexity and die size to a minimum. The single bit stream from the modulator controls a switched current source that is then filtered by three, continuous time resistor-capacitor sections. The capacitors are the only external components that have to be added for standard current-out operation. The filtered current is amplified and mirrored to the supply rail so that the application simply sees a 4 mA–20 mA, 0 mA–20 mA, or 0 mA–24 mA current source output with respect to ground. The AD420 is manufactured on a BiCMOS process that is well suited to implementing low voltage digital logic with high performance and high voltage analog circuitry.

The AD420 can also provide a voltage output instead of a current loop output if desired. The addition of a single external amplifier allows the user to obtain 0 V–5 V, 0 V–10 V, ±5 V, or ±10 V.

The AD420 has a loop fault detection circuit that warns if the voltage at I_{OUT} attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The FAULT DETECT is an active low open drain signal so that one can connect several AD420s together to one pull-up resistor for global error detection. The pull-up resistor can be tied to the V_{LL} pin, or an external +5 V logic supply.

The I_{OUT} current is controlled by a PMOS transistor and internal amplifier as shown in the functional block diagram. The internal circuitry that develops the fault output avoids using a comparator with "window limits" since this would require an actual output error before the FAULT DETECT output becomes active. Instead, the signal is generated when the internal amplifier in the output stage of the AD420 has less than approximately one volt remaining of drive capability (when the gate of the output PMOS transistor nearly reaches ground). Thus the FAULT DETECT output activates slightly before the compliance limit is reached. Since the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain, and no output error occurs before the fault detect output becomes active.

The three-wire digital interface, comprising DATA IN, CLOCK, and LATCH, interfaces to all commonly used serial microprocessors without the addition of any external glue logic. Data is loaded into an input register under control of CLOCK and is loaded to the DAC when LATCH is strobed. If a user wants to minimize the number of galvanic isolators in an intrinsically safe application, the AD420 can be configured to run in "asynchronous" mode. This mode is selected by connecting the LATCH pin to Vcc through a current limiting resistor. The data must then be combined with a start and stop bit to "frame" the information and trigger the internal LATCH signal.

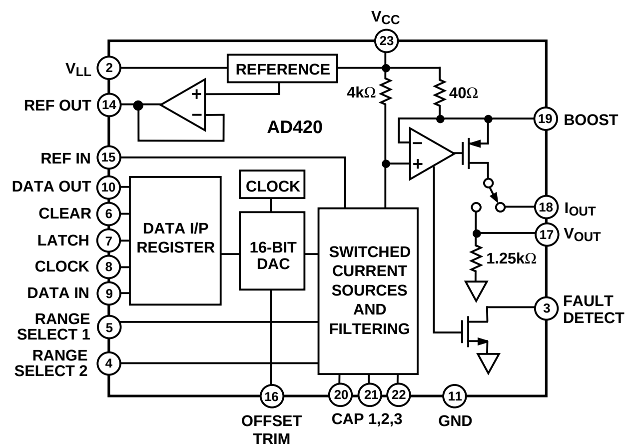


Figure 4. Functional Block Diagram

APPLICATIONS

CURRENT OUTPUT

The AD420 can provide 4 mA–20 mA, 0 mA–20 mA, or 0 mA–24 mA output without any active external components. The three capacitors shown in Figure 5 are all that is required. These can be any type of low cost ceramic capacitors. To meet the specified full-scale settling time of 3 ms, low dielectric absorption capacitors (NPO) are required. Suitable values are C1 = 0.01 μF, C2 = 0.01 μF, and C3 = 0.0033 μF.

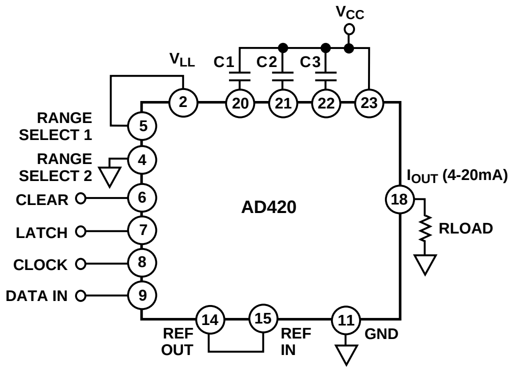


Figure 5. Standard Configuration

DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads connect a 0.01 μF capacitor between I_{OUT} (Pin 18) and GND (Pin 11). This will ensure stability of the AD420 with loads beyond 50 mH. There is no maximum capacitance limit. The capacitive component of the load may cause slower settling, though this may be masked by the settling time of the AD420. A programmed change in the current may cause a back EMF voltage on the output that may exceed the compliance of the AD420. To prevent this voltage from exceeding the supply rails connect protective diodes between I_{OUT} and each of V_{CC} and GND.

VOLTAGE-MODE OUTPUT

Since the AD420 is a single supply device, it is necessary to add an external buffer amplifier to the V_{OUT} pin to obtain a selection of high quality bipolar output voltage ranges as shown in Figure 6.

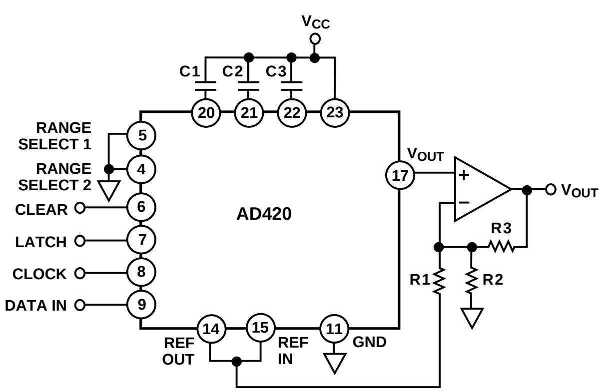


Figure 6.

Table IV. Buffer Amplifier Configuration

R1	R2	R3	V_{OUT}
Open	Open	0	0 V–5 V
Open	R	R	0 V–10 V
R	Open	R	±5 V
R	2R	2R	±10 V

Suitable R = 5 kΩ.

OPTIONAL SPAN AND ZERO TRIM

For those users who would like lower than specified values of offset and gain error, Figure 7 shows a simple way to trim these parameters. Care should be taken to select low drift resistors because they will affect the temperature drift performance of the DAC.

The adjustment algorithm is iterative. The procedure for trimming the AD420 in the 4–20 mA mode can be accomplished as follows:

STEP I . . . OFFSET ADJUST
Load all zeros. Adjust RZERO for 4.00000 mA of output current.

STEP II . . . GAIN ADJUST
Load all ones. Adjust RSPAN for 19.99976 mA (FS – 1 LSB) of output current.

Return to STEP I and iterate until convergence is obtained.

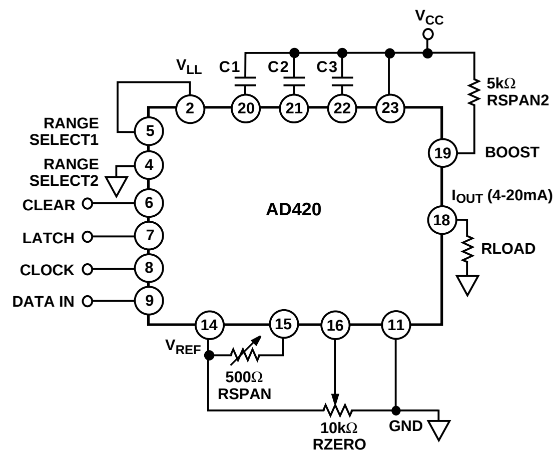


Figure 7. Offset and Gain Adjust

THREE-WIRE INTERFACE

Figure 8 shows the AD420 connected in the three-wire interface mode. The AD420 data input block contains a serial input shift register and a parallel latch. The contents of the shift register are controlled by the DATA IN signal and the rising edges of the CLOCK. Upon request of the LATCH pin the DAC and internal latch are updated from the shift register parallel outputs. The CLOCK should remain inactive while the DAC is updated. Refer to the timing requirements for three-wire interface.

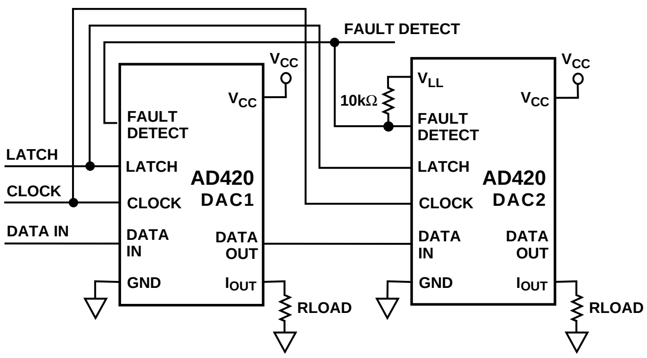


Figure 8. Three-Wire Interface Using Multiple DACs with Joint Fault Detect

USING MULTIPLE DACS WITH FAULT DETECT

The three-wire interface mode can utilize the serial DATA OUT for easy interface to multiple DACs. To program the two AD420s in Figure 8, 32 data bits are required. The first 16 bits are clocked into the input shift register of DAC1. The next 16 bits transmitted pass the first 16 bits from the DATA OUT pin of DAC1 to the input register of DAC2. The input shift registers of the two DACs operate as a single 32-bit shift register, with the leading 16 bits representing information for DAC2 and the trailing 16 bits serving for DAC1. Each DAC is then updated upon request of the LATCH pin. The daisy-chain can be extended to as many DACs as required.

ASYNCHRONOUS INTERFACE USING OPTOCOUPLERS

The AD420 connected in ASYNCHRONOUS INTERFACE mode with optocouplers is shown in Figure 9. Asynchronous operation minimizes the number of control signals required for isolation of the digital system from the control loop. The resistor connected between the LATCH pin and V_{CC} is required to activate this mode. For operation with V_{CC} below 18 V use a 50 kΩ pull-up resistor, from 18 V–32 V use 100 kΩ. Asynchronous mode requires that the clock run at 16 times the data bit rate, therefore to operate at the maximum input data rate of 150 kbps an input clock of 2.4 MHz is required. The actual data rate achieved may be limited by the type of optocouplers chosen. The number of control signals can further be reduced by creating the appropriate clock signal on the current loop side of the isolation barrier.

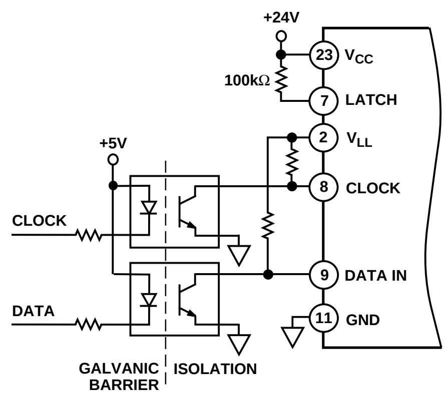


Figure 9. Asynchronous Interface Using Optocouplers

MICROPROCESSOR INTERFACE SECTION

AD420 TO MC68HC11 (SPI BUS) INTERFACE

The AD420 interface to the Motorola SPI (Serial Peripheral Interface) is shown in Figure 10. The MOSI, SCK, and $\overline{SS}$ pins of the HC11 are respectively connected to the DATA IN, CLOCK, and LATCH pins of the AD420. The majority of the interfacing issues are done in the software initialization. A typical routine such as the one shown below begins by initializing the state of the various SPI data and control registers.

```
INIT     LDAA  #$2F       ;SS = 1; SCK = 0; MOSI = 1
         STAA  PORTD      ;SEND TO SPI OUTPUTS
         LDAA  #$38       ;SS, SCK,MOSI = OUTPUTS
         STAA  DDRD       ;SEND DATA DIRECTION INFO
         LDAA  #$50       ;DABL INTRPTS,SPI IS MASTER & ON
         STAA  SPCR       ;CPOL = 0, CPHA = 0, 1MHZ BAUDRATE
NEXTPT   LDAA  MSBY       ;LOAD ACCUM W/UPPER 8 BITS
         BSR   SENDAT     ;JUMP TO DAC OUTPUT ROUTINE
         JMP   NEXTPT     ;INFINITE LOOP
SENDAT   LDY   #$1000     ;POINT AT ON-CHIP REGISTERS
         BCLR  $08,Y,$20  ;DRIVE SS (LATCH) LOW
         STAA  SPDR       ;SEND MS-BYTE TO SPI DATA REG
WAIT1    LDAA  SPSR       ;CHECK STATUS OF SPIE
         BPL   WAIT1      ;POLL FOR END OF X-MISSION
         LDAA  LSBY       ;GET LOW 8 BITS FROM MEMORY
         STAA  SPDR       ;SEND LS-BYTE TO SPI DATA REG
WAIT2    LDAA  SPSR       ;CHECK STATUS OF SPIE
         BPL   WAIT2;     ;POLL FOR END OF X-MISSION
         BSET  $08,Y,$20  ;DRIVE SS HIGH TO LATCH DATA
         RTS
```

The SPI data port is configured to process data in 8-bit bytes. The most significant data byte (MSBY) is retrieved from memory and processed by the SENDAT routine. The $\overline{SS}$ pin is driven low by indexing into the PORTD data register and clear Bit 5. The MSBY is then sent to the SPI data register where it is automatically transferred to the AD420 internal shift resister. The HC11 generates the requisite eight clock pulses with data valid on the rising edges. After the MSBY is transmitted, the least significant byte (LSBY) is loaded from memory and transmitted in a similar fashion. To complete the transfer, the LATCH pin is driven high when loading the complete 16-bit word into the AD420.

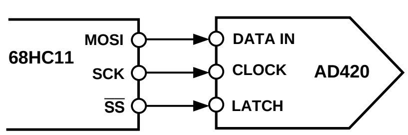


Figure 10. AD420 to 68HC11 (SPI) Interface

AD420 TO MICROWIRE INTERFACE

The flexible serial interface of the AD420 is also compatible with the National Semiconductor MICROWIRE interface. The MICROWIRE interface is used in microcontrollers such as the COP400 and COP800 series of processors. A generic interface to use the MICROWIRE interface is shown in Figure 11. The G1, SK, and SO pins of the MICROWIRE interface are respectively connected to the LATCH, CLOCK, and DATA IN pins of the AD420.

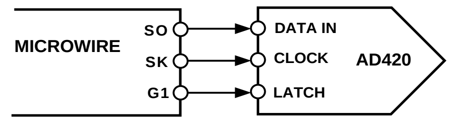


Figure 11. AD420 to MICROWIRE Interface

EXTERNAL BOOST FUNCTION

The external boost transistor reduces the power dissipated in the AD420 by reducing the current flowing in the on-chip output transistor (dividing it by the current gain of the external circuit). A discrete NPN transistor with a breakdown voltage, BV_{CEO}, greater than 32 V can be used as shown in Figure 12.

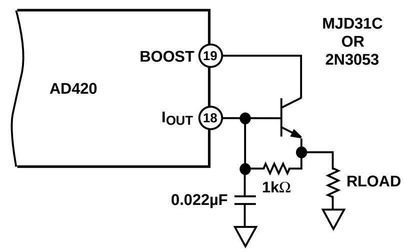


Figure 12. External Boost Configuration

The external boost capability has been developed for those users who may wish to use the AD420, in the SOIC package, at the extremes of the supply voltage, load current, and temperature range. The PDIP package (because of its lower thermal resistance) will operate safely over the entire specified voltage, temperature, and load current ranges without the boost transistor. The plot in Figure 13 shows the safe operating region for both package types. The boost transistor can also be used to reduce the amount of temperature induced drift in the part. This will minimize the temperature induced drift of the on-chip voltage reference, which improves drift and linearity.

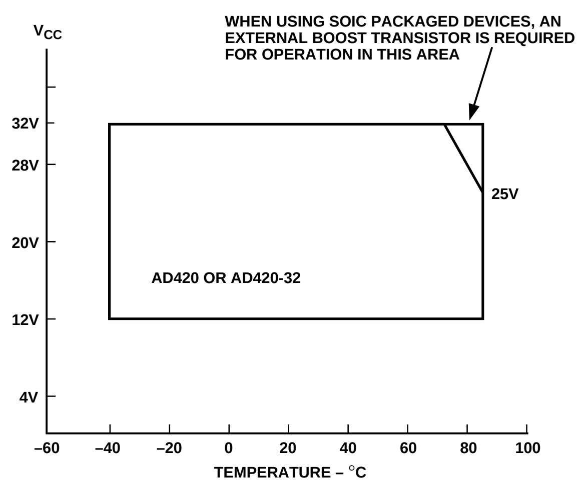


Figure 13. Safe Operating Region

AD420 PROTECTION

TRANSIENT VOLTAGE PROTECTION

The AD420 contains ESD protection diodes which prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. In order to protect the AD420 from excessively high voltage transients such as those specified in IEC 801, external power diodes and a surge current limiting resistor may be required, as shown in Figure 14. The constraint on the resistor is that during normal operation the output voltage level at I_{OUT} must remain within its voltage compliance limit

$$(I_{OUT} \times (Rp + R_{LOAD}) \leq V_{CC} - 2.5\ V)$$

and the two protection diodes and resistor must have appropriate power ratings.

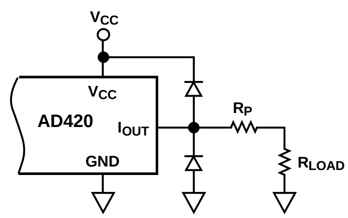


Figure 14. Output Transient Voltage Protection

BOARD LAYOUT AND GROUNDING

The AD420 ground pin, designated GND, is the "high quality" ground reference point for the device. Any external loads on the REF OUT and V_{OUT} pins of the AD420 should be returned to this reference point. Analog and digital ground currents should not share a common path. Each signal should have an appropriate analog or digital signal return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths.

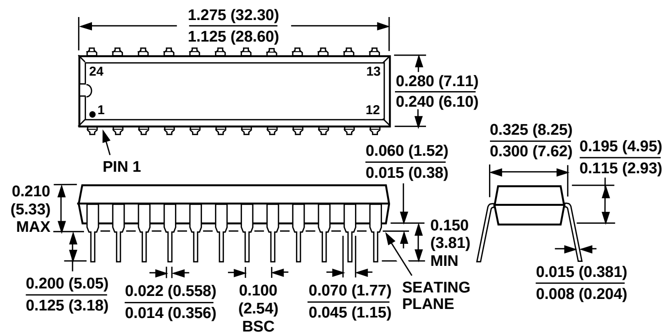
POWER SUPPLIES AND DECOUPLING

The AD420 supply pins, V_{CC} (Pin 23) and V_{LL} (Pin 2), should be decoupled to GND with 0.1 µF capacitors to eliminate high frequency noise that may otherwise get coupled into the analog system. High frequency ceramic capacitors are recommended. The decoupling capacitors should be located in close proximity to the pins and the ground line to have maximum effect.

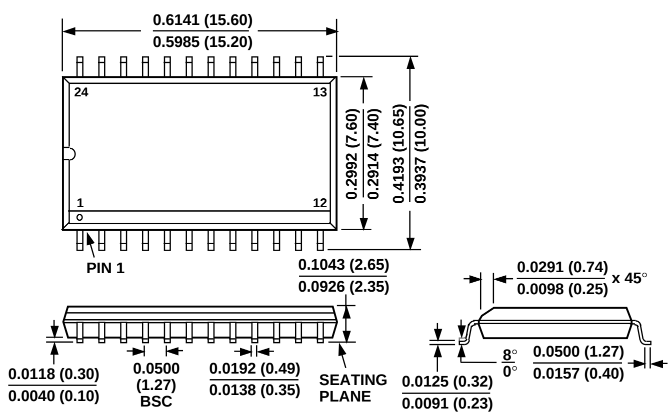
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

N-24
24-Lead Plastic DIP



R-24
24-Lead Small Outline (SOIC)



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